

CLAIMS

What is claimed is:

- 1 1. A method, comprising:
 - 2 receiving a legacy type hardware interrupt request (“IRQ”) by a processor during
 - 3 a native mode runtime of the processor; and
 - 4 servicing the legacy type hardware IRQ received during the native mode runtime,
 - 5 wherein the native mode runtime is a higher performance state of the processor than a
 - 6 legacy mode runtime of the processor defined by a number of bits processed in parallel.

- 1 2. The method of claim 1, further comprising:
 - 2 transitioning from the native mode runtime to the legacy mode runtime in
 - 3 response to the legacy type hardware IRQ to service the legacy type hardware IRQ.

- 1 3. The method of claim 2 wherein servicing the legacy type hardware IRQ
2 includes:
 - 3 executing at least one legacy type interrupt service routine (“ISR”); and
 - 4 returning to the native mode runtime prior to servicing another legacy type
 - 5 hardware IRQ.

- 1 4. The method of claim 3 wherein servicing the legacy type hardware IRQ
2 includes servicing the legacy type hardware IRQ with at least one legacy type ISR
3 invoked by a native type ISR.

1 5. The method of claim 3, further comprising:
2 copying the at least one legacy type ISR from a firmware unit to system memory;
3 and
4 servicing the legacy type hardware IRQ with the copied at least one legacy type
5 ISR executed from the system memory.

1 6. The method of claim 1, further comprising:
2 receiving a native type hardware IRQ by the processor during the legacy mode
3 runtime of the processor;
4 transitioning from the legacy mode runtime to the native mode runtime in
5 response to the native type hardware IRQ; and
6 servicing the native type hardware IRQ.

1 7. The method of claim 1 wherein the legacy type hardware IRQ includes an IRQ
2 from a hardware entity that executes 16-bit code and wherein the legacy mode runtime of
3 the processor includes executing 16-bit code by the processor.

1 8. The method of claim 1 wherein the native type hardware IRQ includes an IRQ
2 from an entity that executes one of 32-bit code and 64-bit code and wherein the native
3 mode runtime of the processor includes executing one of 32-bit code and 64-bit code by
4 the processor.

1 9. The method of claim 1, further comprising:
2 receiving a legacy type hardware IRQ by the processor during the legacy mode
3 runtime;
4 transitioning to the native mode runtime in response to the legacy type hardware
5 IRQ to determine a type of the legacy type hardware IRQ;
6 transitioning back to the legacy type hardware IRQ; and
7 servicing the legacy type hardware IRQ during the legacy mode runtime of the
8 processor.

1 10. A machine-accessible medium that provides instructions that, if executed by a
2 machine, will cause the machine to perform operations comprising:
3 receiving a legacy type hardware interrupt request (“IRQ”) by a processor of the
4 machine during a native mode runtime of the processor; and
5 servicing the legacy type hardware IRQ received during the native mode runtime,
6 wherein the native mode runtime is a higher performance state of the processor than a
7 legacy mode runtime of the processor defined by a number of bits processed in parallel.

1 11. The machine-accessible medium of claim 10, further embodying instructions
2 that, if executed by the machine, will cause the machine to perform operations, further
3 comprising:
4 transitioning from the native mode runtime to the legacy mode runtime in
5 response to the legacy type hardware IRQ to service the legacy type hardware IRQ..

1 12. The machine-accessible medium of claim 11, further embodying instructions
2 that, if executed by the machine, will cause the machine to perform the operations
3 wherein servicing the legacy type hardware IRQ includes:
4 executing at least one legacy type interrupt service routine (“ISR”); and
5 returning to the native mode runtime prior to servicing another legacy type
6 hardware IRQ.

1 13. The machine-accessible medium of claim 12, further embodying instructions
2 that, if executed by the machine, will cause the machine to perform the operations
3 wherein:
4 servicing the legacy type hardware IRQ includes servicing the legacy type
5 hardware IRQ with at least one legacy type ISR invoked by a native type ISR.

1 14. The machine-accessible medium of claim 12, further embodying instructions
2 that, if executed by the machine, will cause the machine to perform operations, further
3 comprising:
4 copying the at least one legacy type ISR from a firmware unit to system memory;
5 and
6 servicing the legacy type hardware IRQ with the copied at least one legacy type
7 ISR executed from the system memory.

1 15. The machine-accessible medium of claim 10, further embodying instructions
2 that, if executed by the machine, cause the machine to perform operations, further
3 comprising:

4 receiving a native type hardware IRQ by the processor during the legacy mode
5 runtime of the processor;
6 transitioning from the legacy mode runtime to the native mode runtime in
7 response to the native type hardware IRQ; and
8 servicing the native type hardware IRQ.

1 16. The machine-accessible medium of claim 10, further embodying instructions
2 that, if executed by the machine, cause the machine to perform the operations wherein the
3 legacy type hardware IRQ includes an IRQ from a hardware entity that executes 16-bit
4 code and wherein the legacy mode runtime of the processor includes executing 16-bit
5 code by the processor.

1 17. The machine-accessible medium of claim 10, further embodying instructions
2 that, if executed by the machine, cause the machine to perform the operations wherein the
3 native type hardware IRQ includes an IRQ from an entity that executes one of 32-bit
4 code and 64-bit code and wherein the native mode runtime of the processor includes
5 executing one of 32-bit code and 64-bit code by the processor.

1 18. The machine-accessible medium of claim 10, further embodying instructions
2 that, if executed by the machine, cause the machine to perform operations, further
3 comprising:

4 receiving a legacy type hardware IRQ by the processor during the legacy mode
5 runtime;

6 transitioning to the native mode runtime in response to the legacy type hardware
7 IRQ to determine a type of the legacy type hardware IRQ;

8 transitioning back to the legacy type hardware IRQ; and

9 servicing the legacy type hardware IRQ during the legacy mode runtime of the
10 processor.

1 19. A processing system, comprising

2 a processor to receive a first native type hardware interrupt request (“IRQ”) and to
3 receive a first legacy type hardware IRQ during a native mode runtime of the processor;

4 and

5 a flash memory unit communicatively coupled to the processor and having stored
6 therein at least one legacy type ISR, the processor to execute the at least one legacy type
7 ISR in response to the legacy type hardware IRQ, wherein the native mode runtime is a
8 higher performance state of the processor than a legacy mode runtime of the processor
9 defined by a number of bits processed in parallel.

1 20. The processing system of claim 19 wherein the processor to transition from
2 the native mode runtime to the legacy mode runtime in response to the legacy type
3 hardware IRQ and prior to executing the at least one legacy type ISR.

1 21. The processing system of claim 20 wherein the processor to return to the
2 native mode runtime after executing the at least one legacy type ISR and prior to
3 executing another legacy type ISR in response to another legacy type hardware IRQ.

1 22. The processing system of claim 20 wherein the flash memory unit further
2 having stored therein a native type ISR, the processor to service the first legacy type
3 hardware IRQ by executing the at least one legacy type ISR invoked by the native type
4 ISR.

1 23. The processing system of claim 19 wherein the processor further to receive a
2 second native type hardware IRQ during the legacy mode runtime of the processor and
3 wherein the flash memory unit further having stored therein at least one native type ISR,
4 the processor to execute the at least one native type ISR in response to the second native
5 type hardware IRQ.

1 24. The processing system of claim 23 wherein the processor to change from the
2 legacy mode runtime to the native mode runtime in response to the second native type
3 hardware IRQ to execute the at least one native type ISR.

1 25. The processing system of claim 23, further comprising:
2 system memory communicatively coupled to the processor and coupled to receive
3 a copy of the at least one native type ISR and a copy of the at least one legacy type ISR
4 from the flash memory unit, the processor to execute the copy of the at least one native
5 type ISR and the copy of the at least one legacy type ISR from the system memory.

1 26. The processing system of claim 25 wherein the flash memory unit further
2 having stored therein a global interrupt handler, the global interrupt handler to be
3 transferred into system memory, the processor to execute the global interrupt handler in
4 response to either one of the first legacy type hardware IRQ and the first native type
5 hardware IRQ, the global interrupt handler to invoke the copy of the at least one legacy
6 type ISR in response to the first legacy type hardware IRQ and to invoke the copy of the
7 at least one native type ISR in response to the native type hardware IRQ.

1 27. The processing system of claim 19 wherein first legacy type hardware IRQ
2 includes an IRQ from a hardware entity that executes 16-bit code and wherein the legacy
3 mode runtime of the processor includes executing 16-bit code by the processor.

1 28. The processing system of claim 23 wherein the native type hardware IRQ
2 includes an IRQ from an entity that executes one of 32-bit code and 64-bit code and
3 wherein the native mode runtime of the processor includes executing one of 32-bit code
4 and 64-bit code by the processor.